## REMARKS

This Amendment is in response to the Final Office Action mailed November 19, 2003. Applicant has filed a Request for Continued Examination to have the Office withdraw the finality of the Office Action and have this submission entered and considered. In the Office Action, the Examiner rejected claims 1-3, 6-8, 11-13, and 16-18 under 35 U.S.C. § 102. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

### *Rejection Under 35 U.S.C. § 102*

The Examiner rejects claims 1-3, 6-8, 11-13, and 16-18 under 35 U.S.C. § 102(b) as being anticipated by Ross et al. (US 5,915,117).

As per claim 1, the Examiner asserts that Ross discloses a reading a fault deferral indication that is true if faults can be deferred, citing the ITLB.ed entry. Col. 6, lines 48-50.

Applicant has amended claim 1 to provide the element of --reading a fault deferral indication that is true if faults caused by errors in memory values can be deferred--. Applicant respectfully points out that the ITLB.ed entry of Ross is limited to the instruction being executed. Col. 8, lines 5-8. Ross explicitly states that the ITLB.ed is "not associated with the data that is being loaded" [emphasis added]. Col. 8, lines 9-10. Claim 1 has been amended to make clear that the claimed invention is directed to handling errors in the memory values loaded and is thus patentably distinct from the disclosures of Ross.

As per claim 2, the Examiner asserts that Ross discloses the error indication is a flag bit associated with the returned value, citing the PSR.ed value. Col. 10, line 66, through col. 11, line 25. Applicant respectfully disagrees. The PSR.ed value is a bit in the processor status register (PSR) that indicates that the hardware should not reissue the memory reference. Col. 11, lines 4-14. Applicant respectfully submits that PSR.ed is associated with the processor state and not with the returned value as claimed. Applicant has amended claim 2 to provide --associated with the returned memory value-- which further clarifies this distinction.

As per claim 3, applicant relies on the patentability of the claim from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional limitations recited.

As per claims 6-8, these claims are rejected and traversed on the same basis as discussed above for claims 1-3.

As per claims 11-13, these claims are rejected and traversed on the same basis as discussed above for claims 1-3.

As per claims 16-18, these claims are rejected and traversed on the same basis as discussed above for claims 1-3.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-3, 6-8, 11-13, and 16-18 under 35 U.S.C. § 102(b) as being anticipated by Ross.

***Conclusion***

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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By _____

James Henry
Reg. No. 41,064
Tel.: (714) 557-3800 (Pacific Coast)